Amendments to the Claims

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-87. (Cancelled).

88. (Previously presented) Circuitry comprising:

a plurality of monolithic substrates having integrated circuits formed thereon and stacked in layers such that each layer comprises only one of the substrates, wherein at least one of the plurality of substrates is a substantially flexible substrate; and

between adjacent substrates, a bonding layer bonding together the adjacent substrates, the bonding layer being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof.

89. (Previously presented) The apparatus of claim 88, further comprising vertical interconnects having vertical interconnect segments formed of a first metal contact on a first substrate bonded to a second aligned metal contact on a second adjacent substrate.

90. (Previously presented) The apparatus of claim 89, wherein the plurality of aligned vertical interconnect segments are joined to form a vertical interconnect between non-adjacent substrates.

91. (Previously presented) The apparatus of claim 88, wherein at least one of said substrates is a substantially rigid substrate having a first thickness.

92. (Currently amended) The apparatus of claim 91, wherein a plurality of substrates have a reduced second thickness substantially less than said first thickness.

93. (Previously presented) The apparatus of claim 92, wherein a ratio of said first thickness to said second thickness is approximately 10:1.

94. (Currently amended) The apparatus of claim 92, wherein a ratio of said first thickness to said second thickness is at least 10:1.

95. (Currently amended) The ~~method~~ apparatus of claim 88, further comprising vertical interconnects formed between the adjacent bonded substrates to interconnect the integrated circuits in subsequent processing steps.

96. (Currently amended) The ~~method~~ apparatus of claim 88, further comprising vertical interconnects formed between the adjacent bonded substrates to interconnect the integrated circuits in subsequent processing steps.

97. (Previously presented) An integrated circuit structure comprising:

a first substrate having a first surface; and

a second substrate bonded to the first surface of the first substrate to form conductive paths between the first substrate and the second substrate wherein the second substrate is a substantially flexible monolithic monocrystalline semiconductor substrate having active circuitry formed thereon, wherein no other substrates are bonded to the first surface.

98. (Currently amended) The ~~method~~ apparatus of claim 97, wherein the first substrate having polycrystalline active circuitry formed thereon.

99. (Currently amended) The ~~method~~ apparatus of claim 97, wherein the first substrate having active circuitry formed thereon.

100. (Currently amended) The ~~method~~ apparatus of claim 97, wherein at least one of the first and second substrates having passive circuitry formed thereon.

101. (Previously presented) A stacked integrated circuit comprising:

a plurality of integrated circuit substrates having formed on corresponding surfaces thereof complementary patterns of a material bondable using thermal diffusion bonding, wherein at least one of the plurality of substrates is a substantially flexible monolithic integrated circuit substrate; and

a thermal diffusion bonded region between the complementary patterns.

102. (Previously presented) The apparatus of claim 101, wherein at least one integrated circuit substrate of the plurality of integrated circuit substrates has memory circuitry formed thereon, the memory circuitry having a plurality of memory locations including at least one memory location used for sparing, wherein data from the at least one memory location on the at least one integrated circuit substrate that has memory circuitry formed thereon is used instead of data from a defective memory location on the at least one integrated circuit substrate that has memory circuitry formed thereon.

103. (Previously presented) The apparatus of claim 101, wherein at least one integrated circuit substrate of the plurality of integrated circuit substrates has memory circuitry formed thereon and at least one integrated circuit substrate of the plurality of integrated circuit substrates has logic circuitry formed thereon, wherein the at least one integrated circuit substrate that has logic circuitry formed thereon performs programmable gate line address assignment with respect to the at least one integrated circuit substrate that has memory circuitry formed thereon.

104. (Previously presented) The apparatus of claim 101, wherein information processing is performed on data routed between circuitry of at least two of the plurality of integrated circuit substrates.

105. (Previously presented) The apparatus of claim 101, wherein at least one integrated circuit substrate of the

plurality of integrated circuit substrates has reconfiguration circuitry.

106. (Previously presented) The apparatus of claim 101, wherein at least one integrated circuit substrate of the plurality of integrated circuit substrates has logic circuitry formed thereon for performing at least one function from the group consisting of: virtual memory management, ECC, indirect addressing, content addressing, data compression, data decompression, graphics acceleration, audio encoding, audio decoding, video encoding, video decoding, voice recognition, handwriting recognition, power management and database processing.

107. (Previously presented) The apparatus of claim 101, further comprising:

a memory array having a plurality of memory storage cells, a plurality of data lines, and a plurality of gate lines, each memory storage cell stores a data value and has circuitry for coupling that data value to one of the plurality of data lines in response to receiving a gate control signal from one of the plurality of gate lines;

circuitry that generates the gate control signal in response to receiving an address, including means for mapping addresses to gate lines; and

a controller that determines if one of the plurality of memory cells is defective and alters the mapping to eliminate references to the one of the plurality of memory cells that is defective.

108. (Previously presented) The apparatus of claim 101, further comprising:

at least one controller substrate having logic circuitry formed thereon;

at least one memory substrate having memory circuitry formed thereon;

a plurality of data lines and a plurality of gate lines on each memory substrate;

an array of memory cells on each memory substrate, each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting of one of the plurality of gate lines;

a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment; and

controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

109. (Previously presented) The apparatus of claim 108, wherein said controller substrate logic:

tests the array of memory cells periodically to determine if one of said memory cells is defective; and

removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines.

110. (Previously presented) The apparatus of claim 108, further comprising programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines.

111. (Previously presented) The apparatus of claim 108, wherein the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order, wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell.

112. (Previously presented) The apparatus of claim 108, wherein:

the logic circuitry of the at least one controller substrate is tested by an external means; and

the array of memory cells of the at least one memory substrate are tested by the logic circuitry of the at least one controller substrate, wherein the testing achieves a functional testing of a substantial portion of the array of memory cells.

113. (Previously presented) The apparatus of claim 108, wherein the logic circuitry of the at least one controller substrate performs functional testing of a substantial portion of the array of memory cells.

114. (Previously presented) The apparatus of claim 108, wherein the controller substrate logic is further configured to:

prevent the use of at least one defective gate line; and

replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line.

115. (Previously presented) The apparatus of claim 108, wherein the controller substrate logic is further configured to prevent the use of at least one defective gate line.

116. (Previously presented) The apparatus of claim 108, wherein the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate.

117. (Previously presented) The apparatus of claim 101, wherein at least one of the plurality of integrated circuit substrates is a thinned substantially flexible substrate.

118 (Previously presented) The apparatus of claim 88, wherein the circuitry is formed with a low stress dielectric.

119. (Previously presented) The apparatus of claim 118, wherein the low stress dielectric is at least one of a silicon dioxide dielectric and caused to have stress of about $5x10^8$ dynes/cm^2 or less.

120. (Previously presented) The apparatus of claim 101, wherein at least one of the plurality of integrated circuit substrates is formed with a low stress dielectric.

121. (Previously presented) The apparatus of claim 120, wherein the low stress dielectric is at least one of a silicon dioxide dielectric and caused to have a stress of about $5x10^8$ dynes/cm^2 or less.

122. (Previously presented) The apparatus of claim 97, wherein at least one of the first substrate and the second substrate is a thinned substantially flexible substrate.

123. (Previously presented) The apparatus of claim 97, further comprising a low stress dielectric layer overlying at least one of the first substrate and the second substrate.

124. (Previously presented) The apparatus of claim 123, wherein the low stress dielectric layer is at least one of a silicon dioxide dielectric and caused to have a stress of about $5x10^8$ dynes cm^2 or less.

125. (Previously presented) The apparatus of claim 97, wherein at least one substrate of the first and second substrates has memory circuitry formed thereon, the memory circuitry having a plurality of memory locations including at least one memory location used for sparing, wherein data from the at least one memory location on the at least one substrate that has memory circuitry formed thereon is used instead of data from a defective memory location on the at least one substrate that has memory circuitry formed thereon.

126. (Previously presented) The apparatus of claim 97, wherein at least one substrate of the first and second substrates has memory circuitry formed thereon and at least one of the first and second substrates has logic circuitry formed thereon, wherein the at least one substrate that has logic circuitry formed thereon performs programmable gate line address assignment with respect to the at least one substrate that has memory circuitry formed thereon.

127. (Previously presented) The apparatus of claim 97, wherein information processing is performed on data routed between the first and second substrates.

128. (Previously presented) The apparatus of claim 97, wherein at least one substrate of the first and second substrates has reconfiguration circuitry.

129. (Previously presented) The apparatus of claim 97, wherein at least one substrate of the first and second substrates has logic circuitry formed thereon for performing at

least one function from the group consisting of: virtual memory management, ECC, indirect addressing, content addressing, data compression, data decompression, graphics acceleration, audio encoding, audio decoding, video encoding, video decoding, voice recognition, handwriting recognition, power management and database processing.

130. (Previously presented) The apparatus of claim 97, further comprising:

a memory array having a plurality of memory storage cells, a plurality of data lines, and a plurality of gate lines, each memory storage cell stores a data value and has circuitry for coupling that data value to one of the plurality of data lines in response to receiving a gate control signal from one of the plurality of gate lines;

circuitry that generates the gate control signal in response to receiving an address, including means for mapping addresses to gate lines; and

a controller that determines if one of the plurality of memory cells is defective and alters the mapping to eliminate references to the one of the plurality of memory cells that is defective.

131. (Previously presented) The apparatus of claim 97, further comprising:

at least one controller substrate having logic circuitry formed thereon;

at least one memory substrate having memory circuitry formed thereon;

a plurality of data lines and a plurality of gate lines on each memory substrate;

an array of memory cells on each memory substrate, each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting of one of the plurality of gate lines;

a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment; and

controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

132. (Previously presented) The apparatus of claim 131, wherein said controller substrate logic:

tests the array of memory cells periodically to determine if one of said memory cells is defective; and

removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines.

133. (Previously presented) The apparatus of claim 131, further comprising programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines.

134. (Previously presented) The apparatus of claim 131, wherein the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order, wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell.

135. (Previously presented) The apparatus of claim 131, wherein:

the logic circuitry of the at least one controller substrate is tested by an external means; and

the array of memory cells of the at least one memory substrate are tested by the logic circuitry of the at least one controller substrate, wherein the testing achieves a functional testing of a substantial portion of the array of memory cells.

136. (Previously presented) The apparatus of claim 131, wherein the logic circuitry of the at least one controller substrate performs functional testing of a substantial portion of the array of memory cells.

137. (Previously presented) The apparatus of claim 131, wherein the controller substrate logic is further configured to:

prevent the use of at least one defective gate line; and

replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line.

138. (Previously presented) The apparatus of claim 131, wherein the controller substrate logic is further configured to prevent the use of at least one defective gate line.

139. (Previously presented) The apparatus of claim 131, wherein the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate.

140. (Previously presented) The apparatus of claim 118, wherein the stress of the low stress dielectric is tensile.

141. (Previously presented) The apparatus of claim 120, wherein the stress of the low stress dielectric is tensile.

142. (Previously presented) The apparatus of claim 124, wherein the stress of the low stress dielectric is tensile.

143. (Previously presented) The apparatus of claim 88, wherein a major portion of the monolithic substrate is removed.

144. (Previously presented) The apparatus of claim 97, wherein a major portion of the second substantially flexible monolithic monocrystalline semiconductor substrate is removed.

145. (Previously presented) The apparatus of claim 101, wherein a major portion of the at least one substantially flexible monolithic integrated circuit substrate is removed.

146. (New) An integrated circuit structure comprising:

a plurality of semiconductor dice, each die having an integrated circuit formed thereon, said dice being stacked in layers, wherein at least one of the plurality of dice is substantially flexible; and

between adjacent dice, a bonding layer bonding together the adjacent dice, the bonding layer bonding first and second substantially planar adjacent surfaces of the adjacent dice.

147. (New) The apparatus of claim 146, wherein at least one integrated circuit of the plurality of dice is formed with a low stress dielectric.

148. (New) The apparatus of claim 147, wherein the low stress dielectric is at least one of a silicon dioxide dielectric and caused to have stress of about $5x10^8$ dynes/cm^2 or less.

149. (New) The apparatus of claim 147, wherein the stress of the low stress dielectric is tensile.

150. (New) The apparatus of claim 146, wherein at least one of the plurality of dice has a substrate, wherein at least one of a major portion of the substrate is removed and a major portion of the substrate is able to be removed while retaining the structural integrity of the integrated circuit formed on the substrate.

151. (New) The apparatus of claim 146, wherein at least one of the plurality of dice is a substantially rigid substrate having a first thickness.

152. (New) The apparatus of claim 152, wherein at least one of the plurality of dice has a second thickness, wherein the second thickness is substantially less than the first thickness.

153. (New) The apparatus of claim 146, further comprising at least one of interconnects formed between adjacent bonded surfaces of adjacent dice and wire interconnects formed between the dice.

154. (New) The apparatus of claim 146, wherein information processing is performed on data routed between any two of the plurality of dice.

155. (New) The apparatus of claim 146, wherein at least one of the plurality of dice having at least one of polycrystalline active circuitry formed thereon, reconfiguration circuitry formed thereon and passive circuitry formed thereon.

156. (New) An integrated circuit structure comprising:

a substrate having a first surface; and

a semiconductor die having an integrated circuit formed thereon bonded to the first surface of the substrate with conductive paths between the substrate and the die wherein the die is a substantially flexible.

157. (New) The apparatus of claim 156, wherein the integrated circuit is formed with a low stress dielectric.

158. (New) The apparatus of claim 157, wherein the low stress dielectric is at least one of a silicon dioxide dielectric and caused to have stress of about $5x10^8$ dynes/cm^2 or less.

159. (New) The apparatus of claim 157, wherein the stress of the low stress dielectric is tensile.

160. (New) The apparatus of claim 156, wherein the substrate having circuitry formed thereon.

161. (New) The apparatus of claim 156, wherein the substrate is formed from a non-semiconductor material.

162. (New) The apparatus of claim 156, wherein the die has a substrate, wherein at least one of a major portion of the substrate of the die is removed and a major portion of the die is able to be removed while retaining the structural integrity of the integrated circuit formed on the die.

163. (New) The apparatus of claim 156, wherein the conductive paths are at least one of wire interconnects and interconnects formed on the bonded surfaces between the substrate and the die.

164. (New) The apparatus of claim 156, wherein information processing is performed on data routed between the substrate and the die.

165. (New) The apparatus of claim 156, wherein at least one of the substrate and die having at least one of polycrystalline active circuitry formed thereon, die has reconfiguration circuitry formed thereon and passive circuitry formed thereon.